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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 15

Application Number: 09/397,952
Filing Date: September 17, 1999
Appellant(s): AHMAD, AFTAB

Tina Chen
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on November 17, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct. Claims 1,3,5,7-15,23, and 25-28 as recited in Appellants' brief –Appendix B are pending after entry of the amendments filed with this Appeal brief.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is deficient because the as-filed disclosure only supports the following :

(Reproduced below is the Applicants' summary of the invention along with clarifications by examiner presented in underline and unsupported applicants' additions surrounded in parentheisis , ()).

The present invention relates generally to techniques for improving hot carrier resistance of a transistor gate in a semiconductor substrate .

The scale of integration of semiconductor devices has increased significantly , and more devices have been positioned on smaller sized silicon substrates. As devices have become smaller, the channel length of the devices have become so small that functional problems result. In particular, source/drain punch through and hot electron susceptibility are two such problems . Source/drain punch through results in lack of gate control over the transistor and causes significant current leakages. The problem may be reduced by positioning anti punch through implants, such as Boron for n-Channel devices and Phosphorous or Arsenic for p-channel devices, that prevent depletion regions from meeting (in the channel region).

Hot electron susceptibility, which is defined as the injection of high energy electrons in to the gate oxide layer and farther into the polysilicon forming the gate of the CMOS structure, severely reduces the threshold voltage of the transistor. Hot electron susceptibility may be reduced by oxidizing the gate edge next to the (source and) drain regions by conventional source/drain reoxidation described as a thermal spacer growth step carried out to form an oxide layer 130 over the source/drain regions . The spacer growth step can also be performed using any of the known techniques in the art. This spacer growth step is a heating step, like a conventional post-doping thermal drive step (specification page 5 lines 4-5, 14-15 and 24-25) thereby rounding the gate edges and increasing the gate oxide thickness at the gate edges. However, in ULSI applications, the oxide is not a (very) good dielectric for the higher electric fields in these applications.

Lightly doped drain (LDD) structures are also used to overcome hot electron susceptibility. In a LDD structure, the source/drain regions are formed by implanting two different ions with different doping densities. A lightly doped drain region which are uniquely designed drain structures adjacent a channel region separates the channel region from a heavily doped drain region, and the lightly doped region significantly reduces the high electric filed that causes hot electron injection in to the gate oxide. However, ever-decreasing device dimensions have brought many constrains to conventional LDD process technologies.

A proper LDD drain should provide adequate hot-carrier protection for the device. In CMOS technology Nitrogen implantation into the source/drain regions during the formation of NMOSFET and PMOSFET prior to the formation of the sidewall spacer (SiO_2) has been used for this purpose. The implanted nitrogen atoms are then segregated after the spacer deposition at the interface between the substrate and by a low temperature treatment, thereby forming a silicon nitride layer under the sidewall spacer, which can suppress the hot electron injection. However, this technique limits the nitrogen atom segregation to the area under the sidewall spacer. Due to the high electric field strength, the structure cannot suppress the hot (electron) carrier injection into the gate oxide as the nitrogen segregated area (tends to) only covers the region under the CVD deposited SiO_2 sidewall spacer.

The present invention provides a processing technique that is capable of reducing punch trough and hot electron susceptibility in smaller devices. The claimed

invention is a process that improves hot carrier resistance of a transistor gate by isolating oxide region positioned on the wafer and a polysilicon layer positioned thereon (by isolating the gate polysilcion with a nitride film) . In the preferred process, nitrogen is globally implanted into the substrate and nitrogen doped region 118 are formed in the source and drain regions 117 of the substrate 101. The source and drain regions are subsequently reoxidized to oxidize exposed portions of the gate polysilicon 112 and the source and drain regions117. Under the oxidation conditions, a ploysilicon bird's beak region124 forms and nitrogen atoms diffuse into the gate region to form silicon nitride. During the oxide growth, the oxide layer 130 can extend laterally under the ploysilicon gate edges and form a wedge shaped oxide profile at the gate edges (due to the particular sequenced used – actually oxide extensions are formed during any oxide growth process irrespective of the sequence used). The diffusion of nitrogen atoms into the oxidized gate edges advantageously forms silicon nitride under the gate edges. As is well known, silicon nitride is an excellent dielectric and therefore provides effective protection against current leakage into the gate polysilicon.

Each of the pending ... after implanting nitrogen.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct.

(7) Grouping of Claims

The brief contains a statement that all pending claims stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix B to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

US 5,405,701	Ahmad et al.	April 11, 1995
US 5,972,783	Arai et al.	Oct. 26, 1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-15 and 23 –28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (U.S. Patent No. 5,405,791 hereinafter Ahmad) previously applied and in view of Arai et al. (U. S. Patent No. 5,972,783 herein after Arai).

With respect to claim 1, Ahmad describes a process of forming a gate structure on a semiconductor substrate including: providing a semiconductor substrate having a channel region formed therein so as to define source and a drain region (Ahmad fig. 5(A), identical to steps shown in applicants' figures 1-2 etc. and described in the specification pages 4 to 6), and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric (Ahmad fig. 5 (A)).

Ahmad does not specifically describe implanting nitrogen in to said substrate .

Arai in fig. 1(b), etc. and col. 12 lines 45-63 describes implanting nitrogen in to said substrate to better control the crystallinity thereby reducing transistor degradation and provide a transistor with better performance and reliability.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Arai's implantation step in Ahmad's process to better control the crystallinity thereby reducing transistor degradation to provide a transistor .with better performance and reliability. (Arai col. 13 lines 60-64).

The remaining limitations of claim1 are :

Conducting a source/drain reoxidation, thereby forming a sidewall spacer after implanting nitrogen . (Ahmad fig. 2, col. 3 Lines 53-57).

With respect to claim 3, wherein the substrate comprises silicon. (Ahmad col. 3 line 31) .

With respect to claim 5, wherein implanting nitrogen with greater than 10 raised to 12 nitrogen atoms. (Arai col. 12 lines 62-63).

With respect to claim 8, wherein oxidizing said portion further comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer . (Ahmad fig. 4 # 22 and Arai fig. 1 (b) # 5a).

With respect to claims 9 and 10 wherein conducting said source/drain reoxidation comprises forming a nitride layer on the semiconductor substrate and wherein the nitride layer laterally extends under at least a portion of the conductive layer. (Ahmad figure 2 and col. 3 lines 63-64).

With respect to claim 11, wherein the gate dielectric comprises silicon oxide (Ahmad col. 3 line 51).

With respect to claim 12, wherein a second sidewall spacer is deposited over the sidewall spacer. (Ahmad figure 4).

With respect to claim 13, it repeats the steps of claims 1-12 stated above and further adds a protective layer over the source and rain regions, said protective layer comprising said insulator element and characterized by a dielectric constant higher than that of silicon oxide (Ahmad col. 3 lines 64 – silicon nitride layer).

With respect to claim 14, it repeats the steps of claims 8-10 and 13 and is rejected for reasons set out above.

With respect to claim 15 it repeats the steps of claim 1 ,6 and 8 and is rejected for reasons set out under claims 1,4,6and 8.

With respect to claim 23, Ahmad and Arai describe a process of eliminating hot electron injection into a gate electrode positioned on a gate oxide adjacent a channel interposed between a source and a drain region in a silicon substrate, the process

comprising : forming a nitrogen doped region in said source and drain regions by nitrogen implantation (Arai fig. 19b) etc.) , forming silicon nitride film over a portion of said gate electrode so that a portion of said silicon nitride film penetrates under said gate electrode during said forming step wherein said portion of said silicon nitride film prevents hot electron injection into said gate electrode wherein forming said silicon nitride film includes conducting a source/drain reoxidation after forming said nitrogen doped region (Ahmad col. 3 line 56 to col. 4 line 5). (Ahmad fig. 2, col. 3 Lines 53-57).

With respect to claim 24, wherein forming the silicon nitride film comprises exposing the gate electrode to an oxidizing ambient (Ahmad col. 4 lines 5-9, ozone atmosphere) .

With respect to claim 26, wherein an insulation layer is deposited over the gat electrode . (Ahmad fig. 3) and an isotropically etching said insulating layer to form sidewall spacers . (Ahmad col. 6 lines 3 to 10).

With respect to claim 27, wherein the source/drain is implanted. (Ahmad fig. 5).

With respect to claim 28, further comprising lightly doping said source and rain regions to grade a junction between said channel and said source and rain regions. (Ahmad figs. 8 to 10, and Arai fig. 2(d) ,etc.) .

(11) Response to Argument (in the Appeal brief)

A. A prima facie case of Obviousness has been established by the rejections.

Appellants' contend that the Examiner has not shown any teaching or suggestion in the cited art to combine the individual elements (sic. method steps) in the manner

claimed in the instant invention. Particularly the sequence of steps recited in the claims is not taught or suggested by the prior art .

Applicants' contention that the particular sequence namely : Implanting nitrogen into said substrate ; and conducting a source/drain reoxidation, thereby forming a sidewall spacer after implanting said nitrogen. (claims 1, 13 , 15 23 – all pending independent claims in relevant parts) is not taught by the applied art is not supported by facts.

The applied Ahmad reference describes all the steps recited in claim 1 including an ion implatation step (at least figure 1 to form N-well and P-well) followed by source/drain reoxidation at least in figure 2 and col. 2 lines 53 to col. 4 line 2 (reproduced below) :

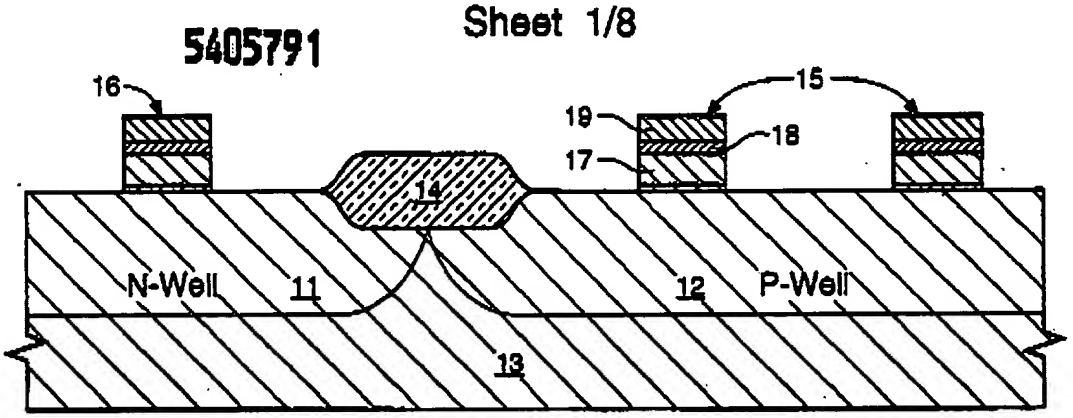


FIG. 1

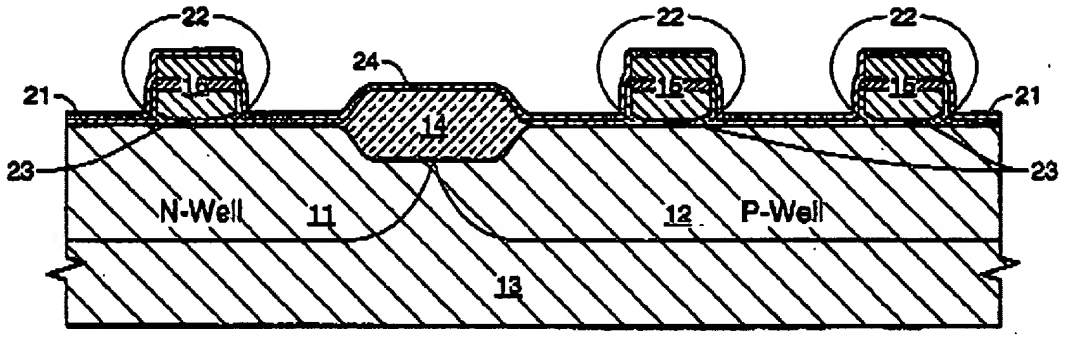


FIG. 2

Referring now to FIG. 2, the in-process circuitry of FIG. 1 has been subjected to a source/drain reoxidation step which has formed a thermal oxide layer 21 on the surface of the source/drain regions and on the sidewalls of both N-channel and P-channel transistor gates. The reoxidation step also causes the formation of a slight bird's beak structure 22 under both edges of each transistor gate, which lowers the lateral electric field strength in N-channel transistor drain regions, thereby reducing hot electron injection into the gate oxide layer 23. Following the reoxidation step, a layer of silicon nitride dielectric etch-stop layer 24 is blanket deposited over the in-process circuitry. Other materials, which are selectively etchable with respect to silicon dioxide, may be substituted for the silicon nitride etch-stop layer 24. Although dielectric materials are preferred, polysili-

4

con may also be used if later removed to protect against shorting between devices.

(The above quotation is reproduced in text format to ensure proper scanning).

" Referring now to Fig. 2, the in-process circuitry of Fig. 1 has been subjected to a source/drain reoxidation step which has formed a thermal oxide layer 21 on the surface of the source/drain regions and on sidewalls of both N-Channel and P-channel transistor gates. The reoxidation step also causes the formation of a slight bird's beak structure 22 under both edges of each transistor gate, which lowers the lateral electric

filed strength in N-channel drain regions, thereby reducing hot electron injection in to gate oxide layer 23. Following the reoxidation step, a layer of silicon nitride dielectric etch-stop layer 24 is blanket deposited over the in-process circuitry. Other materials , which are selectively etchable with respect to silicon di oxide, may be substituted for silicon nitride etch stop layer 24. Although dielectric materials are preferred, poly silicon may also be used if later removed to protect against shorting between devices. "

Ahmad does not specifically mention the ion implanted in its implantation step to be nitrogen but Arai teaches the N implanting step Arai in figures 22 (a) –22 (d) describing prior art shows (reproduced below.):

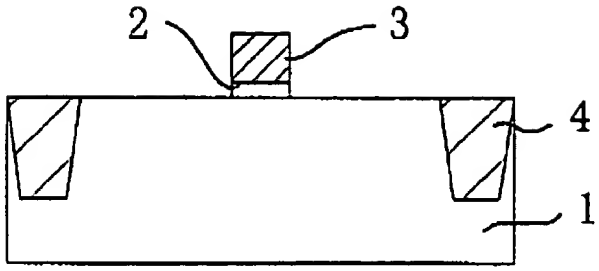


Fig. 22(a)
PRIOR ART

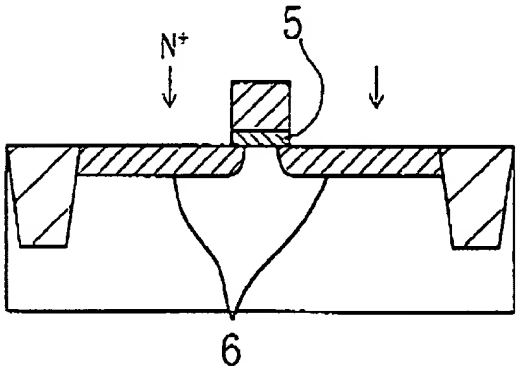


Fig. 22(b)
PRIOR ART

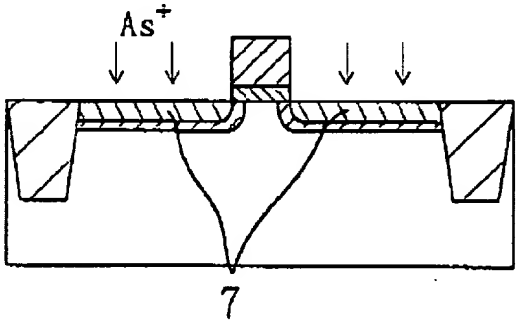


Fig. 22(c)
PRIOR ART

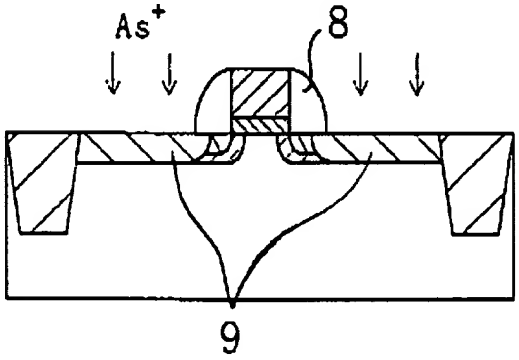


Fig. 22(d)
PRIOR ART

Therefore the prior art as taught by Arai includes a process wherein the nitrogen is implanted into a substrate as shown in figure 22 (b) and described at least in col. 1 lines 39 to 54 (also reproduced below) :

> Next, in a process step of FIG. 22(*b*), an ion implant is carried out in which ions of nitrogen (N+) are implanted, from above the substrate, into gate electrode 3 and into silicon substrate 1 within the active region. The implanted nitrogen ions are then diffused by an annealing treatment, to simultaneously form oxynitride layer 5 in gate oxide film 2, and nitrogen diffusion layer 6 in a near-surface area of silicon substrate 1.

(The above quotation is reproduced in text format to ensure proper scanning).

" Next in a process step of Fig. 22 (b), an ion implant is carried out in which ions of nitrogen (N+) are implanted, from above the substrate, into gate electrode 3 and into silicon substrate 1, within active region . The implanted nitrogen ions are then diffused by an annealing treatment, to simultaneously from oxynitride layer 5 in gate oxide film and nitrogen diffused layer 6 in a near-surface area of silicon substrate 1."

and the subsequent step of conducting a source/drain reoxidation, (i.e. a thermal spacer growth The thermal spacer growth is further described in Appellants' specification page 6 lines 14 –15 and lines 24-25 as

" The spacer growth step can be performed using any of the known techniques in the art" and " The spacer growth step is a heating step, like a conventional post-doping thermal drive step.".

The applied Arai reference teaches N implantation step (Figure 22 B, etc.) followed by reoxidation (i.e. annealing step , Arai at least in col. 1 lines 46 to53)

Therefore the combination of Ahmad (teaching all the recited steps of claim1 etc. including the ion implantaion step followed by the reoxidation step,)

with Arai's Nitrogen implantation step followed by the reoxidation step, teaches the steps presently recited in the claims in the order recited therein.

The motivation to make the above combination (i.e. substitute Arai's nitrogen implantation for Ahmad's ion implantation in Ahmad's process is provided by Arai at lest in figure 1(b) etc and col. 12 lines 45 to 63 to better control the crystallinity thereby reducing transistor degradation and provide a transistor with better performance and reliability .

Therefore a prima facie showing of obviousness beyond a shadow of doubt has been established by the outstanding rejections including a particular sequence of steps. (i.e. (i) implanting nitrogen into said substrate and (ii) conducting a source/drain reoxidation.

(ii) Reliance on Ex parte Rubin and In re Burhans

Appellants' allege that Rubin and Burhans are inapplicable herein because allegedly their sequence of performing the steps as recited in their claims results in "Unexpected or advantageous" i.e new or unexpected result namely :

It is noted that the cited cases make a exception to their holding only in cases of NEW or UNEXPECTED results not " unexpected or advantageous results " as stated in Appellants' brief.

(a) Appellants' argument that, " An upward motion of implanted nitrogen atoms " as recited in specification page 6 lines 23 –31 is new and

advantageous is not persuasive because Arai in figure 22 (b) and col. 1 lines 46 to 53 states :

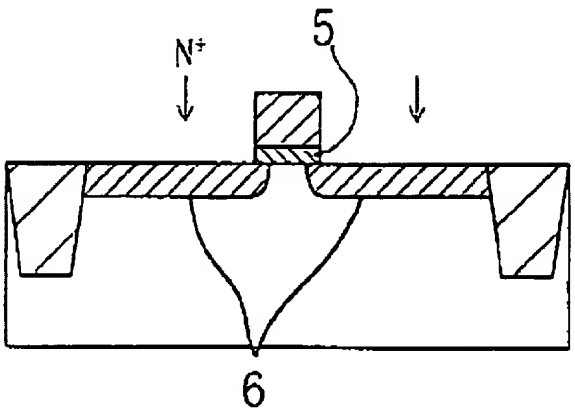


Fig. 22(b)
PRIOR ART

and

Next, in a process step of FIG. 22(*b*), an ion implant is carried out in which ions of nitrogen (N+) are implanted, from above the substrate, into gate electrode 3 and into silicon substrate 1 within the active region. The implanted nitrogen ions are then diffused by an annealing treatment, to simultaneously form oxynitride layer 5 in gate oxide film 2, and nitrogen diffusion layer 6 in a near-surface area of silicon substrate 1.

(The above quotation is reproduced in text format to ensure proper scanning).

" Next in a process step of Fig. 22 (b), an ion implant is carried out in which ions of nitrogen (N+) are implanted, from above the substrate, into gate electrode 3 and into silicon substrate 1, within active region . The implanted nitrogen ions are then diffused by an annealing treatment, to simultaneously from oxynitride layer 5 in gate oxide film and nitrogen diffused layer 6 in a near-surface area of silicon substrate 1."

Therefore it is clear that the Nitrogen ions implanted into the silicon substrate 1 (shown in fig. 22 A) have an upward motion and form oxynitride layer 5 which is above the substrate .

Therefore the alleged new or unexpected result , namely," An upward motion of implanted nitrogen atoms as recited in specification page 6 lines 23 –31 " is neither new nor unexpected and taught by the applied prior art of record.

(b) Appellants' argument that ," the silicon nitride formation 131 also extends laterally at least partially under the gate poly 112 in the region of GBB 124 due to mobility of atoms during oxidation and form a nitride edge portion at least partially underlying the gate " is new and advantageous is not persuasive because Ahmad in col.1 line 36 and lines 50-55 state :

> channel with the silicon crystal lattice. Hot electron injection can be reduced by oxidizing the gate edge near the drain. This not only increases gate oxide layer thick-

and

> tion. As spacers are designed to have sufficient height and density to trap ions which are being implanted directly above them, a spacer will result in ions being implanted in a region of the substrate that is offset from the gate edge a distance that is equal to the width of the spacer.

(The above quotation is reproduced in text format to ensure proper scanning).

" channel with the silicon crystal lattice. Hot electron injection can be reduced by oxidizing the gate edge near the drain. This not only increases gate oxide layer thickness "

and

" ... As spacers are designed to have sufficient height and density to trap ions which are being implanted directly above them , a spacer will result inions being

implanted in a region of the substrate that is Offset from the gate edge a distance that is equal to the width of the spacer."

and Arai in figure 1(a) and col. 12 lines 55 to 58 state :

Fig. 1(a)

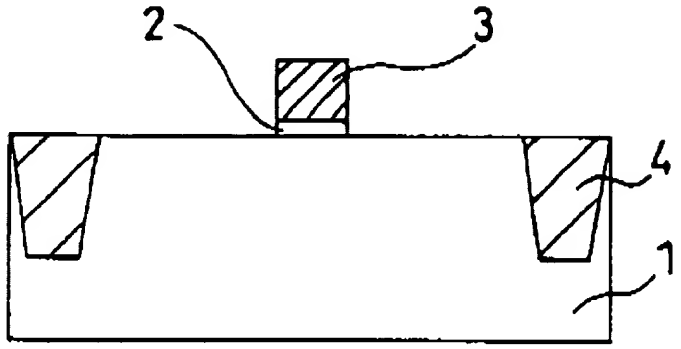
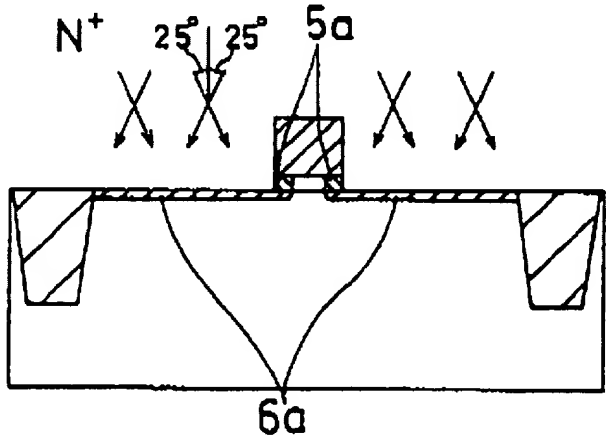


Fig. 1(b)



Thereafter, the nitrogen ions are diffused by an annealing treatment, whereby oxynitride layer **5***a* is formed at each edge of gate oxide film **2** and nitrogen diffusion layer **6***a* is formed in silicon substrate **1**. A preferred implant energy

(The above quotation is reproduced in text format to ensure proper scanning).

" Thereafter, the nitrogen ions are diffused by an annealing treatment , whereby oxynitride layer 5 a is formed at each edge of gate oxide film 2 and nitrogen diffusion layer 6a is formed in silicon substrate 1. A preferred implant energy "..

As seen in the above figure when nitrogen ions are implanted in to silicon substrate 1 a silicon nitride layer 6 at least partially extending under gate poly (2,3 seen in figure 1 a) are formed by the mobility (diffusion) of the Nitrogen ions when annealed (i.e. during oxidation) .

Therefore the alleged new or unexpected result , namely," the silicon nitride formation 131 also extends laterally at least partially under the gate poly 112 in the region of GBB 124 due to mobility of atoms during the oxidation extension of the silicon nitride formation under the gate poly " is neither new nor unexpected and taught by the prior art of record.

(c) Appellants' argument that the silicon nitride formation 131 also extends partially at least partially under the gate poly 112 in the region of GBB 124 due to mobility of atoms during oxidation extension of the silicon nitride formation under the gate poly effectively minimizes the high electric field induced current leakages into the gate poly 112 (emphasis supplied) is new and advantageous is not persuasive because Ahmad in col. 1 lines 35-36 states :

> channel with the silicon crystal lattice. Hot electron injection can be reduced by oxidizing the gate edge near the drain. This not only increases gate oxide layer thick-

and Arai 13 lines 35 to 42 states :

> formed only at both edges of gate oxide film 2. A major cause of hot carrier degradation exists in the fact that hot carriers are captured in a gate oxide film on the drain side. Accordingly, the formation of oxynitride layer 5a at at least one of the edges of gate oxide film 2 (oxynitride is formed at each edge of gate oxide film 2 in the present embodiment), prevents the occurrence of hot carrier degradation.

(The above quotation is reproduced in text format to ensure proper scanning).

" channel with the silicon crystal lattice> Hot electron injection can be reduced by oxidizing the gate edge near the drain. This not only increases gate oxide layer thickness "

and

" formed only at both edges of gate oxide film 2. A major cause of hot carrier degradation exists in the fact that hot carriers are captured in a gate oxide film on the drain side . Accordingly, the formation of oxynitride layer 5a at at least one of the edges of gate oxide film 2 (oxynitride is formed at each edge of gate oxide film 2 in the present embodiment), prevents the occurrence of hot carrier degradation ".

Therefore the alleged new or unexpected result , namely," the silicon nitride formation 131 also extends partially at least partially under the gate poly 112 in the region of GBB 124 due to mobility of atoms during oxidation extension of the silicon nitride formation under the gate poly effectively minimizes the high electric field induced current leakages into the gate poly 112 " is neither new nor unexpected and taught by the prior art of record.

(d) Appellants' argument that the silicon nitride formation 131 also extends partially at least partially under the gate poly 112 in the region of GBB 124 due to mobility of atoms during oxidation extension of the silicon nitride formation under the gate poly and tends to limit the nitride formation to the region under the deposited sidewall spacer. " (emphasis supplied)) is new and advantageous is not persuasive because Ahmad in figure 2 and col. 3 lines 63 states :

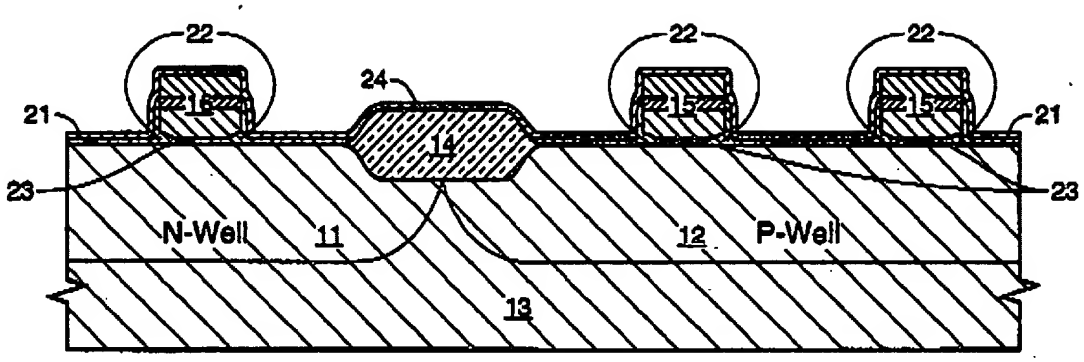


FIG. 2

Referring now to FIG. 2, the in-process circuitry of FIG. 1 has been subjected to a source/drain reoxidation step which has formed a thermal oxide layer 21 on the surface of the source/drain regions and on the sidewalls of both N-channel and P-channel transistor gates. The reoxidation step also causes the formation of a slight bird's beak structure 22 under both edges of each transistor gate, which lowers the lateral electric field strength in N-channel transistor drain regions, thereby reducing hot electron injection into the gate oxide layer 23. Following the reoxidation step, a layer of silicon

(The above quotation is reproduced in text format to ensure proper scanning).

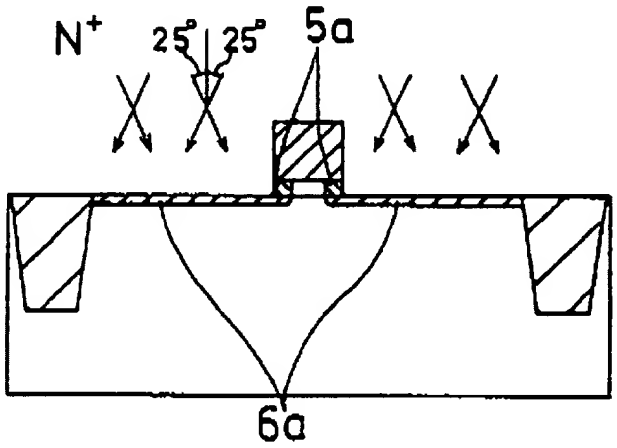
" Referring now to Fig. 2, the in-process circuitry of Fig. 1 has been subjected to a source/drain reoxidation step which has formed a thermal oxide layer 21 on the surface of the source/drain regions and on sidewalls of both N-Channel and P-channel transistor gates. The reoxidation step also causes the formation of a slight bird's beak structure 22 under both edges of each transistor gate, which lowers the lateral electric filed strength in N-channel drain regions, thereby reducing hot electron injection in to gate oxide layer 23. Following the reoxidation step, a layer of silicon "

It is clear from above that the reoxidation step causes a nitride layer 22 to be formed only at the edge of the gates , in other words only below the deposited sidewall

spacer (i.e. limit nitride formation to the region under the deposited sidewall spacer) which isolates the lower poly silicon gate edges from the neighboring source/drain regions and thus reduces hot electron injection .

and Arai in figure 1 (b) and col. 13 lines 13 states :

Fig. 1 (b)



and

sistor having an oxynitride layer. More specifically, in the present nMOS field effect transistor, oxynitride layer **5***a* is formed only at both edges of gate oxide film **2**. A major cause of hot carrier degradation exists in the fact that hot carriers are captured in a gate oxide film on the drain side. Accordingly, the formation of oxynitride layer **5***a* at at least one of the edges of gate oxide film **2** (oxynitride is formed at each edge of gate oxide film **2** in the present embodiment), prevents the occurrence of hot carrier degradation.

(The above quotation is reproduced in text format to ensure proper scanning).

" sistor having an oxynitride layer. More specifically in the present nMOS field effect transistor, oxynitride layer 5 a is formed only at both edges of gate oxide film 2. A major cuase of hot carrier degradation exists in the fact that hot carriers are captured in a gate oxide film on the drain side. Accordingly, the formation of oxynitride layer 5a at at least one of the edges of gate oxide film 2 (oxynitride is formed at each edge of gate

oxide film 2 in the present embodiment), prevents the occurrence of hot carrier degradation. "

It is clear from above that the reoxidation step causes a oxynitride layer 5a to be formed only at each edge of the gates(i.e. limit the nitride formation to the region under the deposited sidewall spacer) which isolates the lower poly silicon gate edges from the neighboring source/drain regions and thus reduces hot electron injection .

Thus all of the alleged unexpected and advantageous results are neither new or unexpected because they are also disclosed the applied Ahmad and Arai references as shown above.

The examiner has clearly acknowledged the specific sequence of steps recited in the pending claims and further clearly pointed the sections of the applied Ahmad and Arai references that in combination teach the process in which nitrogen implantation is followed by source/drain oxidation.

(ii) Arai teaches source/drain reoxidation.

Appellants' allegation that Arai does not teach any source/drain reoxidation is not persuasive for the following reasons :

It is noted that Appellant's specification describes a thermal spacer growth step while the claims recite this same step as source/drain reoxidation and at other times as source/drain oxidation.

It is well settled law that Appellants' claims must be given the broadest reasonable interpretation. (See In re Pearson, 181 USPQ 641 (CCPA 138).

It is also noted that Appellant's specification at least in page 6 describes the following :

" Referring to Figure 3, following the Nitrogen implantation step, a thermal spacer growth step is carried out to form oxide layer 130 over the source / drain regions 117 and on the sidewall 122 of both n-channel 106A and p-channel 106B transistor gates. "

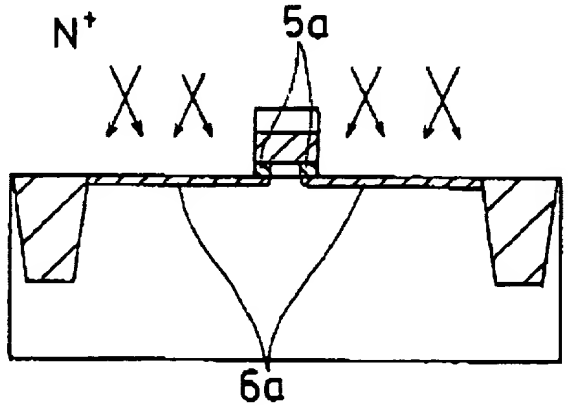
" The spacer growth step can be performed using any of the known techiniques in the art. " (page 6 lines 14-15) .

" The spacer growth step is a heating step, like a conventional post-doping thermal drive step. " (page 6 lines 24-25).

Therefore according to Appellants' description in their specification the recited source/drain reoxidation step is a thermal spacer growth/deposition step growing a oxide layer over the source/drain regions and the sidewall of the transistor gates , further this step can be performed by using any of the known techniques like a post-doping thermal drive step, etc.

Arai in figs.2(b) , etc. shows oxide layers 5a and 6a being formed over the gate and sidewalls (spacers) (5a) and over the source/drain regions 6a.

Fig. 2(b)



Therefore it is clear that Arai teaches / describes source./drain reoxidation which is also known as conventional post-doping thermal drive step (i.e Arai's nitrogen implantation (conventional doping step) followed by an annealing treatment (i.e. post doping thermal drive step – col. 12 lines 55-60 driving doped nitrogen ions) and can be performed using any of the known techniques in the art (thermal drive by annealing) , to achieve the same end results.

Appellants' argument that Ahmad does not teach nitrogen implantation and Arai does not teach any source/drain oxidation (which is incorrect for reasons set out above) and since neither reference includes both steps, it is clear that the sequence of nitrogen implantation followed by source/drain oxidation is not taught by the references (is also incorrect because for reasons stated above Arai teaches both steps of nitrogen implantation followed by source/drain oxidation) , further Appellants' above analysis is based upon impermissible piecemeal attacks on references that cannot show nonobviousness where as herein the rejections are based on combinations of references. (See In re Keller, 208 USPQ 871, CCPA 1981).

Appellants' argument that the Examiner must show that the prior art provides reasonable expectation that nitrogen implantation followed by source/drain reoxidation would be successful in forming a sidewall spacer for the purpose of improving hot carrier resistance of a transistor buy isolating the gate polysilicon with a nitride film is not persuasive for the following reasons :

(a) It is agreed that the prior art must show "art provides reasonable expectation that nitrogen implantation followed by source/drain reoxidation would be

successful in forming a sidewall spacer ' , but as the claims presently do not recite The limitation , "for the purpose of improving hot carrier resistance of a transistor by isolating the gate polysilicon with a nitride film " this limitation should not be given patentable weight.

As shown above the applied prior art namely Ahmad (teaching ion implantation followed by source/drain reoxidation) and Aria (N implantation followed by reoxidation) further both U.S. patents are presumed to be valid and must be afforded the full faith and credit for reasonable expectation of success.

As shown above Further Arai shows describes nitrogen implantation (figure 1 (b) , etc.) followed by source/drain reoxidation forming a sidewall spacer (Aria col. 12 lines 55-60, etc. and Ahmad in col. 3 lines 53 to col. 4 line 2, etc. shows ion implantation to form source/drain followed by source/drain reoxidation) .

Assuming arguendo that the limitation , "for the purpose of improving hot carrier resistance of a transistor buy isolating the gate polysilicon with a nitride film " is recited in the claims , Arai at least in col. 13 lines 35-43 and Ahmad in at least col. 1 lines 35-37, etc. teach this non –recited limitation.

Thus fulfilling the alleged standard (In re Dow Chemicals) of finding the suggestion to combine (both steps are recited in single Arai paten and Arai in col.) and the expectation of success (single Arai reference teaches both steps therefore both steps have been successfully done).

Therefore it is not necessary to look to Appellants' disclosure.

Therefore none of the Appellants' arguments are persuasive .

For the above reasons , it is believed that the rejections should be sustained.

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